An RV32IM Processor with a Fuzzy Logic Branch Prediction Unit and Selective Execution

The Reduced Instruction Set Computer V (RISC-V) 32-bit architecture with an Integer base instruction set and Multiplication and Division extension (RV32IM) is widely adopted in embedded systems; however, pipeline control hazards limit its performance. Conventional branch prediction techniques exhibit limited accuracy under complex, irregular control-flow patterns. This work proposes the integration of the Fuzzy Logic Branch Prediction Unit (FLBPU) into a five-stage RV32IM pipeline. The FLBPU uses an adaptive fuzzy inference system, considering instruction type and global branch history, to calculate prediction confidence dynamically. This confidence metric controls speculative execution via a Selective Execution Technique (SET). The design also incorporates a hazard control unit and enhanced dependency analysis. On a Xilinx Zynq UltraScale+ Field-Programmable Gate Array (FPGA) at 100 MHz, the design was tested with 83 instructions executed over 135 cycles, achieving an Instructions Per Cycle (IPC) of 0.615. The FLBPU processed 32 branch instructions, predicting all 32 branches with 26 correct predictions and 6 mispredictions, yielding an 18.75% misprediction rate and 81.25% branch prediction accuracy. Accuracy progression was observed as follows: branches one to four had 0% accuracy during the initial learning phase; branches five to fifteen showed gradual improvement from 0% to 60% accuracy; branch 24 reached 75% accuracy; and branch 32 achieved 81.25% accuracy. Post-synthesis hardware utilization was 3,385 Lookup Tables (LUTs), 5,387 Flip-Flops (FFs), and 5 Digital Signal Processing (DSP) blocks, with an on-chip power consumption of 0.309 W.

Keywords:
RISC-V, branch prediction, fuzzy logic, adaptive systems, FPGA implementation, pipeline hazards, embedded processors, computer architecture